**PATENT** 

Makoto Ono, et al.

Application No.: 10/004,168

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**IN THE ABSTRACT:** 

Please replace the Abstract with the following amended Abstract:

A method and system are provided for analyzing defects having the potential to become electrical failures, during the inspection of particles and/or pattern defects of a wafer used in the manufacture of electronic devices such as semiconductor integrated circuits. Defect map data is processed along with failure probability data. Next, defect-dependent failure probability calculations are made to obtain the failure probability of each defect in the defect map data. That data is then used to prepare failure-probability-added defect map data. Further, a selection process of defects to be reviewed is used to reorder and filter defects from the failure-probability-added defect map data, thus selecting one or more defects for review.

## **REMARKS**

The specification has been replaced pursuant to M.P.E.P. §608.01(q). No new matter has been added. The Abstract has been replaced.

The claims have been canceled and replaced with new claims.

## **CONCLUSION**

All claims now pending in this Application are believed to be in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Reg. No. 37,478

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